

MC74VHCT00A

Quad 2-Input NAND Gate

The MC74VHCT00A is an advanced high speed CMOS 2-input NAND gate fabricated with silicon gate CMOS technology. It achieves high speed operation while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHCT00A input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74VHCT00A to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

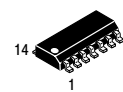
- High Speed: $t_{PD} = 5.0$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2.0$ V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 3.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: 48 FETs or 12 Equivalent Gates



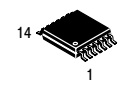
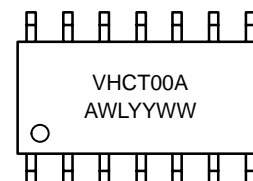
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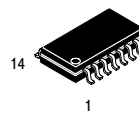
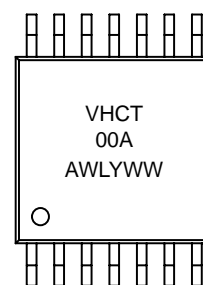
MARKING DIAGRAMS



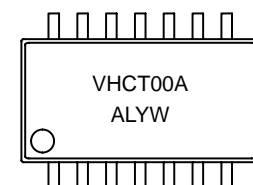
SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



SOIC EIAJ-14
M SUFFIX
CASE 965



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT00AD	SOIC-14	48 Units/Rail
MC74VHCT00ADR2	SOIC-14	2500 Units/Reel
MC74VHCT00ADT	TSSOP-14	96 Units/Rail
MC74VHCT00ADTEL	TSSOP-14	2000 Units/Reel
MC74VHCT00ADTR2	TSSOP-14	2000 Units/Reel
MC74VHCT00AM	SOIC EIAJ-14	48 Units/Rail
MC74VHCT00AMEL	SOIC EIAJ-14	2000 Units/Reel

MC74VHCT00A

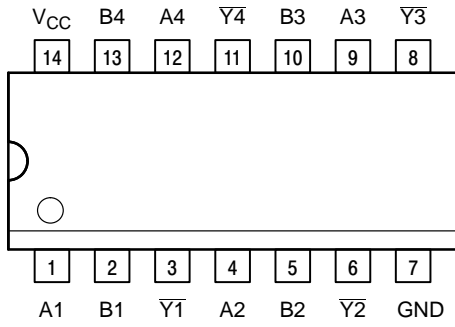


Figure 1. Pin Assignment
(Top View)

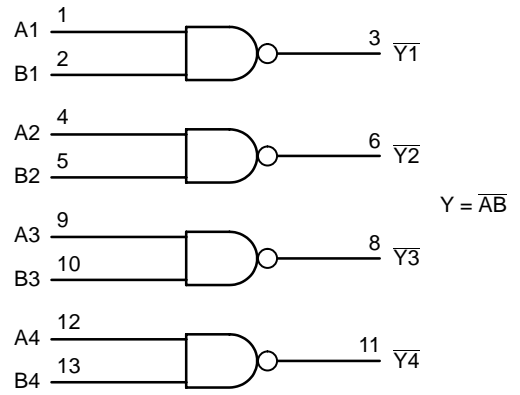


Figure 2. Logic Diagram

PIN ASSIGNMENT	
1	IN A1
2	IN B1
3	OUT $\bar{Y}1$
4	IN A2
5	IN B2
6	OUT $\bar{Y}2$
7	GND
8	OUT $\bar{Y}3$
9	IN A3
10	IN B3
11	OUT $\bar{Y}4$
12	IN A4
13	IN B4
14	V _{CC}

FUNCTION TABLE

Inputs		Output
A	B	\bar{Y}
L	L	H
L	H	H
H	L	H
H	H	L

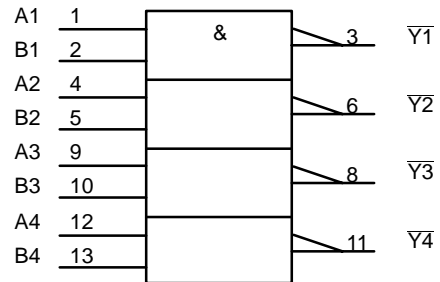


Figure 3. IEC LOGIC DIAGRAM

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MAXIMUM RATINGS (Note 1.)

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	-0.5 to 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current V _{OUT} < GND; V _{OUT} > V _{CC}	+20	mA
I _{OUT}	DC Output Current, per Pin	+25	mA
I _{CC}	DC Supply Current, V _{CC} and GND	+50	mA
P _D	Power Dissipation in Still Air, SOIC Packages (Note 2.) TSSOP Package (Note 2.)	500 450	mW
T _L	Lead temperature, 1 mm from case for 10 s	260	°C
T _{stg}	Storage temperature	-65 to +150	°C
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 3.) Machine Model (Note 4.) Charged Device Model (Note 5.)	> 2000 > 200 > 3000	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and Below GND at 125°C (Note 6.)	±300	mA

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

- Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
- Derating
 - SOIC Packages: -7 mW/°C from 65° to 125°C
 - TSSOP Package: -6.1 mW/°C from 65° to 125°C
- Tested to EIA/JESD22-A114-A
- Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	DC Supply Voltage	3.0	5.5	V
V _{IN}	DC Input Voltage	0.0	5.5	V
V _{OUT}	DC Output Voltage V _{CC} = 0 High or Low State	0.0 0.0	5.5 V _{CC}	V
T _A	Operating Temperature Range	-55	+125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

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The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

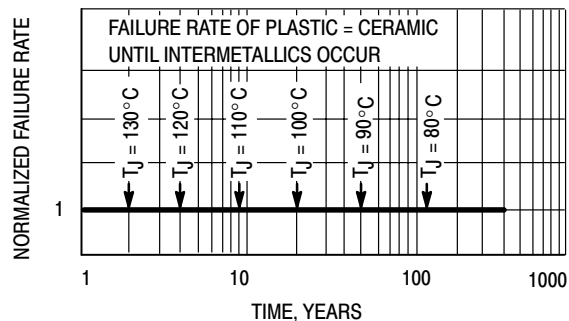


Figure 4. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	Minimum High-Level Input Voltage		3.0	1.4			1.4		1.4		V
			4.5	2.0			2.0		2.0		
			5.5	2.0			2.0		2.0		
V_{IL}	Maximum Low-Level Input Voltage		3.0			0.53		0.53		0.53	V
			4.5			0.8		0.8		0.8	
			5.5			0.8		0.8		0.8	
V_{OH}	Minimum High-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50 \mu\text{A}$	3.0	2.9	3.0		2.9		2.9		V
		4.5	4.4	4.5		4.4		4.4			
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0	2.58			2.48		2.34		V
		4.5	3.94			3.80		3.66			
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50 \mu\text{A}$	3.0		0.0	0.1		0.1		0.1	V
		4.5		0.0	0.1		0.1		0.1		
V_{OL}	Maximum Low-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0			0.36		0.44		0.52	V
		4.5			0.36		0.44		0.52		
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			2.0		20		40	μA
I_{CCT}	Quiescent Supply Current	Input: $V_{IN} = 3.4 \text{ V}$	5.5			1.35		1.50		1.65	mA
I_{OPD}	Output Leakage Current	$V_{OUT} = 5.5 \text{ V}$	0.0			0.5		5.0		10	μA

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AC ELECTRICAL CHARACTERISTICS $C_{load} = 50 \text{ pF}$, Input $t_r = t_f = 3.0 \text{ ns}$

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A \leq 85^\circ\text{C}$		$T_A \leq 125^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Maximum Propagation Delay, Input A or B to Y	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		4.1 5.5	10.0 13.5		11.0 15.0		13.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		3.1 3.6	6.9 7.9		8.0 9.0		9.5 10.5	
C_{IN}	Maximum Input Capacitance			5.5 10			10		10	pF

Symbol	Parameter	Typical @ 25°C , $V_{CC} = 5.0 \text{ V}$		Unit
		Min	Max	
C_{PD}	Power Dissipation Capacitance (Note 7.)	17		pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$, $C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \text{ V}$, Measured in SO Package)

Symbol	Characteristic	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	-0.4	-0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

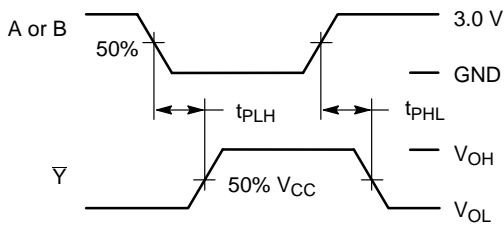
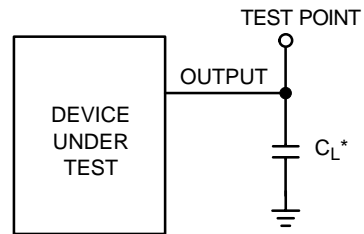


Figure 5. Switching Waveforms



*Includes all probe and jig capacitance

Figure 6. Test Circuit

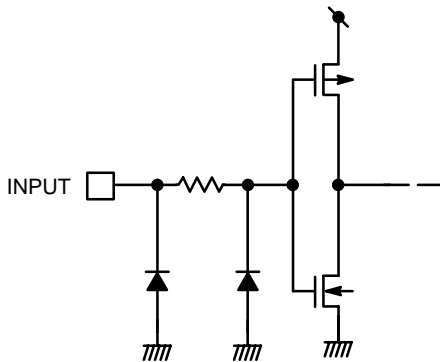
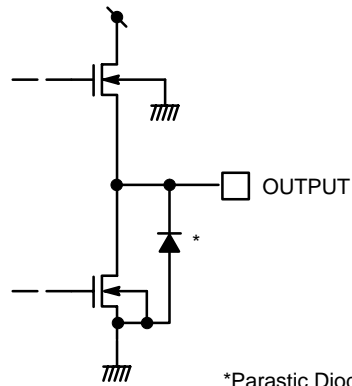


Figure 7. Input Equivalent Circuit



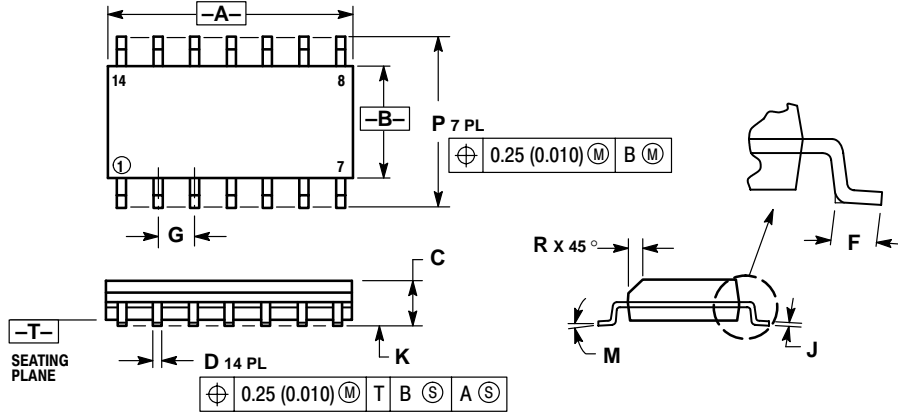
*Parasitic Diode

Figure 8. Output Equivalent Circuit

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PACKAGE DIMENSIONS

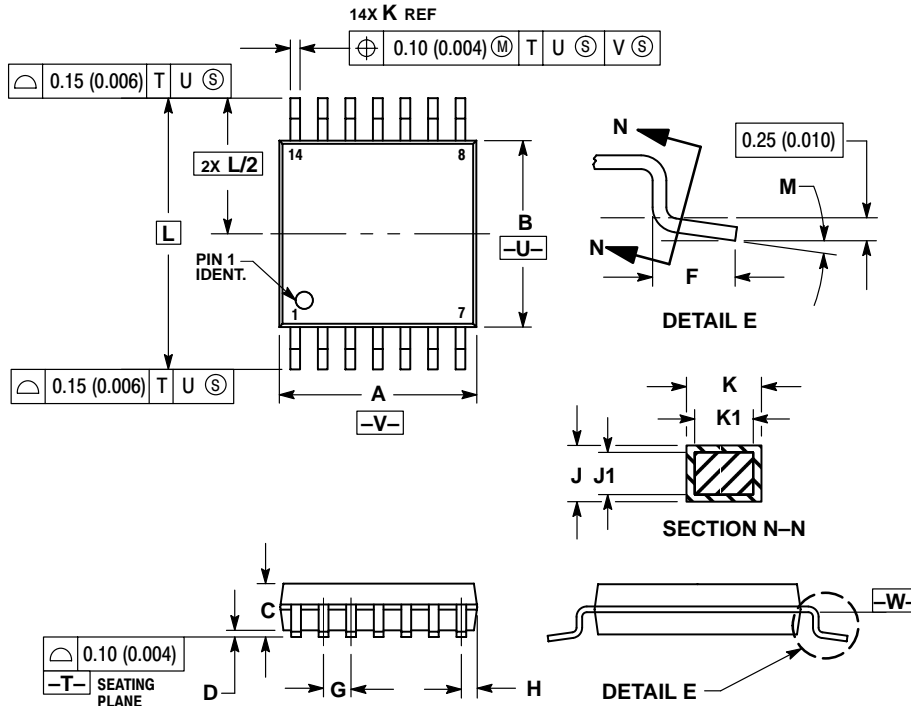
D SUFFIX SOIC PACKAGE CASE 751A-03 ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX TSSOP PACKAGE CASE 948G-01 ISSUE O

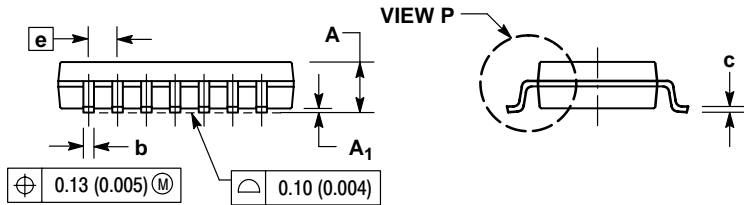
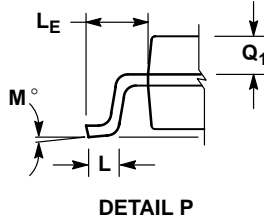
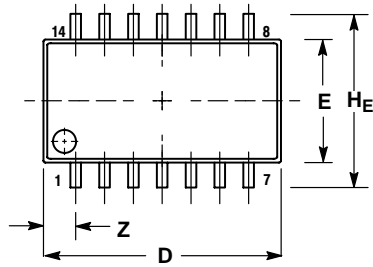


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHCT00A

M SUFFIX
SOIC EIAJ PACKAGE
CASE 965-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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